CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor device, the method comprising the steps of:

forming a charge trapping layer over a substrate;

forming doped regions in the substrate; and

forming buried bitlines in the doped regions resulting in a doped region forming adjacent to at least one of the buried bitlines,

wherein the doped region adjacent the at least one of the buried bitlines inhibits a leakage current between the buried bitlines.

2. The method according to claim 1, further including the step of:

defining at least two regions in the charge trapping layer for programming and erasing the semiconductor device.

3. The method according to claim 1, further including the step of:

forming a conductive layer over the charge trapping layer,

wherein the charge trapping layer is interposed between the substrate and the conductive layer.

4. The method according to claim 1, wherein the charge trapping layer is a multi-layer dielectric layer.

5. The method according to claim 4, wherein the multi-layer dielectric layer includes a charge trapping dielectric layer.

6. The method according to claim 5, wherein the multi-layer dielectric layer is an oxide-nitride-oxide (ONO) layer.

7. The method according to claim 1, wherein the charge trapping layer includes:

a tunneling layer;

a charge trapping dielectric layer; and

an insulating layer;

wherein the tunneling layer is disposed over the substrate, the charge trapping dielectric layer is disposed over the tunneling layer and the insulating layer is disposed over the charge trapping dielectric layer.

8. The method according to claim 7, wherein a material of the tunneling layer is one or more of a SiO_2 or an oxynitride.

9. The method according to claim 8, wherein the charge trapping layer includes one or more materials of a permittivity greater than SiO_2.

10. The method according to claim 9, wherein the one or more materials are one or more of, silicon nitride (Si_xN_y), silicon oxynitride (SiO_xN_y), aluminum oxide (Al_2O_3), hafnium oxide (HfO), zirconium oxide (ZrO), titanium oxide (TiO), yttrium oxide (YO), zirconium silicate, hafnium silicate, lanthanum oxide (La_2O_3), cerium oxide (CeO_2), bismuth silicon oxide ($Bi_4Si_2O_{12}$), tantalum oxide (Ta_2O_5), tungsten oxide (WO_3), $LaAlO_3$, BST ($Ba_{1-x}Sr_xTiO_3$), $PbTiO_3$, $BaTiO_3$, $SiTiO_3$, $PbZrO_3$, PST ($PbSc_xTa_{1-x}O_3$), PZN ($PbZn_xNb_{1-x}O_3$), PZT ($PbZr_xTi_{1-x}O_3$), PMN ($PbMg_xNb_{1-x}O_3$) or the like.

11. The method according to claim 1, further including the steps of:

forming a hard mask layer over the charge trapping layer;

depositing and patterning a photoresist layer over the hard mask layer to form a pattern in the photoresist; and

transferring the pattern from the photoresist to the hard mask layer.

12. The method according to claim 11, wherein the first dopant type is boron and the second dopant type is arsenic.

13. The method according to claim 11, further including the steps of:

implanting the substrate through apertures in the hard mask to form the doped region adjacent the at least one of the buried bitlines with a first dopant type, and

implanting the substrate through the apertures in the hard mask to form the buried bitlines of a second dopant type opposite the first dopant type.

14. The method according to claim 13, further including the steps of:

forming an insulating layer over the hard mask layer, and

planarizing the insulating layer such that the insulating layer fills apertures in the hard mask layer.

15. The method according to claim 14, further including the step of:

removing the hard mask layer.

16. The method according to claim 11, further including the step of:

annealing the semiconductor device to repair damage in the charge trapping layer due to the implanting of the first dopant type.

17. The method according to claim 1, wherein the charge trapping layer is a conducting layer.

18. The method according to claim 1, further including the step of:

forming a control gate over the charge trapping layer.

19. The method according to claim 18, further including the step of:

forming a multi-layer dielectric layer over the charge trapping layer,

wherein the multi-layer dielectric layer is interposed between the charge trapping layer and the control gate.

20. A semiconductor device, comprising:

a substrate;

buried bitlines formed in the substrate;

a doped region formed adjacent at least one of the buried bitlines;

a charge trapping layer disposed over the substrate; and

a conductive layer disposed over the charge trapping layer,

wherein the doped region adjacent the least one of the buried bitlines inhibits a leakage current between the buried bitlines.